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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

THEODORE W. HOUSTON

Serial No. 10/054,957 (ti-25000.1)

Filed January 25, 2002

For: ASYMMETRICAL DEVICES FOR SHORT GATE
LENGTH PERFORMANCE WITH DISPOSABLE SIDEWALL

Art Unit 2822

Examiner Toniae M. Thomas

Customer No. 23494

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Jay M. Cantor, Reg. No. 19,906

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known pending related appeals and/or interferences though an appeal was filed in Serial No. 09/368,387, the parent of the subject application.

STATUS OF CLAIMS

This is an appeal of claims 10 and 25, all of the rejected claims. No claims have been allowed and Patent No. 6,548,359 has issued for the parent and Patent No. 6,873,008 has issued for a further divisional application. No fee is believed to be required because a Notice of Appeal and a Brief on Appeal were previously filed in this application and the rejection was then withdrawn. However should a fee be required, please charge any costs to Deposit Account No. 20-0668. Claims 1 to 9, 11 to 24 and 26 have been canceled and claims 10 and 25 are being appealed.

STATUS OF AMENDMENTS

An amendment was not filed after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to a transistor which includes, with reference to Figures 4A and 4B, a semiconductor substrate (1) having first and second spaced apart source/drain regions (3, 5) therein and a channel region between the source/drain regions in the substrate having a relatively low V_T central region (27) between the source/drain regions and relatively high controlling V_T regions adjacent to the source/drain regions (29), the channel region having an implanted one of a positive or negative V_T dopant intermediate the source/drain regions and having an implanted one of a negative or positive V_T dopant adjacent the source/drain regions, the opposite of the dopant in the channel region. The controlling V_T is defined as that region which is the least conducting region and that controls the current flow (paragraph {0003}, lines 9 to 12).

As stated in paragraph [0008], as a fourth embodiment (with reference to Figs 4A and 4B), the FET can be made symmetrical rather than asymmetrical as described in the first and second embodiments with a different implant in the center of the channel region relative to the source

and drain ends of the channel region. An implant can be performed following sidewall formation. The sidewalls would then be removed and the entire channel region would be doped n- or p-type to provide either a less heavily net doped region adjacent the source and drain regions if the same conductivity type dopant is used or a more heavily net doped region adjacent the source and drain if the opposite conductivity type dopant is used. The resist pattern used to mask removal of selected sidewalls can also distinguish n- and p-channel transistors for different V_T implants. Optionally, an implant can be performed before formation of the sidewalls, followed by an implant after formation of the sidewalls. For this option, the sidewall can be left in place for formation of the actual gate.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 10 and 25 are anticipated by Jones et al. (U.S. 4,212,683) under 35 U.S.C. 102 (b).

ARGUMENT

Claim 10 was rejected under 35 U.S.C. 102(b) as being anticipated by Jones (U.S. 4,212,683). The rejection is without merit.

It is basic that in order for a rejection under section 102 to be proper, each and every feature of a claim as well as each and every function of each and every feature must be found in a single reference. Clearly, this is not the case as is evident from the fact that the alleged relatively low V_T region referred to by the examiner is region 27 of Jones et al. which extends from source to drain and hence fails to conform to the structure as claimed. Also, claim 10

requires a *central* region of the channel intermediate the controlling regions which is not found in Jones et al.

More specifically, claim 10 requires, among other features, a semiconductor substrate having first and second spaced apart source/drain regions therein and a channel region between the source/drain regions in the substrate *having a relatively low V_T central region between the source/drain regions and relatively high controlling V_T regions adjacent to the source/drain regions*, the channel region having an implanted one of a positive or negative V_T dopant intermediate the source/drain regions and having an implanted one of a negative or positive V_T dopant adjacent the source/drain regions, the opposite of the dopant in the central region mentioned above. The controlling V_T is defined as that region which is the least conducting region and thus controls the current flow.

This claim refers to the fourth embodiment as discussed on pages 5 and 9 of the specification. No such features are taught or suggested by Jones either alone or in the total combination as claimed. The term "controlling V_T is defined at page 3, lines 10ff as that region which is the least conducting region and thus controls the current flow. Nothing in Jones et al. defines the regions 28, 29 as performing that function and no reason is stated in Jones et al. why those regions should perform the function as now claimed. This feature even more clearly defines the invention over the prior art.

Claim 25 depends from claim 10 and therefore defines patentably over Sasaki for at least the reasons set forth as to claim 10.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

10. A transistor which comprises:

(a) a semiconductor substrate having first and second spaced apart source/drain regions therein; and

(b) a channel region between said source/drain regions in said substrate having a relatively low V_T central region between said source/drain regions and relatively high controlling V_T regions adjacent to said source/drain regions, said channel region having an implanted one of a positive or negative V_T dopant intermediate said source/drain regions and having an implanted one of a negative or positive V_T dopant adjacent said source/drain regions, the opposite of said dopant in said central region;

wherein controlling V_T is defined as that region which is the least conducting region and thus controls the current flow.

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Claim 25 (previously added) The transistor of claim 10 wherein said first source/drain region is a source region and said second source/drain region is a drain region.